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10/550,950	09/28/2005	Takaji Numao	12480-000130/US	4086
30/593 7590 03/09/2009 HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910 RESTON, VA 20195				
EXAMINER				
MCCOMMAS, STUART S				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

***Response to Arguments***

1. Applicant's arguments filed 2/13/2009 have been fully considered but they are not persuasive.

On pages 11-12 of Applicant's remarks, Applicant argues that Kimura does not disclose a second capacitor and that the transistor in Dawson is not a driving transistor as recited in the claim.

The Examiner respectfully disagrees, because Kimura clearly discloses a second capacitor 1811 in figure 18. Simply because other limitations of this capacitor are disclosed in Dawson does not mean that Kimura does not disclose a second capacitor which meets the claimed limitations cited in the previous Office Action. Further Dawson does disclose that transistor 365 is a driving transistor in column 5 lines 15-31.

On pages 12-13, Applicant argues that Kimura and Dawson fail to disclose that during a first period within a current writing period of the driving transistor, the first switching transistor connects the current control terminal to the current output terminal, the second switching transistor disconnects the second terminal and the current output terminal from each other, and the third switching transistor connects the second terminal to the predetermined voltage line.

The Examiner respectfully disagrees, because Dawson discloses that during a first period within a current writing period of the driving transistor (365) the first switching transistor (370) connects the current control terminal to the current output terminal (column 4 lines 41-67; column 5 lines 1-31; figure 3), and Kimura discloses that during a first period within a current writing period of the driving transistor the second switching

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transistor (1818) disconnects the second terminal and the current output terminal from each other (figures 18-19), and that the third switching transistor (1807) connects the second terminal to the predetermined voltage line (figures 18-19). These operations can happen at any time during a first period within a current writing period, and they could happen simultaneously or consecutively and thus Kimura does disclose the invention as claimed.